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## Paper ID [A0210]

(Please fill this Paper ID in OMR Sheet)

# BCA (205) (S05) (O) (Sem. - 2<sup>nd</sup>) DIGITAL CIRCUITS AND LOGIC DESIGN

Time: 03 Hours Maximum Marks: 75

#### **Instruction to Candidates:**

1) Section - A is Compulsory.

2) Attempt any Nine questions from Section - B.

#### **Section - A**

 $Q1) (15 \times 2 = 30)$ 

- a) Convert (i) 11011.11(binary number )to decimal number.
  - (ii) 7825.6875 decimal number to octal.
- b) Convert (i) 125.89 binary number to BCD number.
  - (ii) A4F to Octal number.
- c) Simplify

$$(\overline{a+b})+(\overline{a+\overline{b}})$$

d) Prove using truth table

$$A + \overline{A}B = A + B$$

- e) Draw the logic diagram & truth table of Full adder.
- f) Define the term propagation Delay.
- g) Simply the following logic function using k-map and find the minterms & maxterms.

$$F(X,Y,Z) = \overline{X}Z + X\overline{Y}Z + YZ$$

- h) Write the truth table of 3:8 Decoder.
- i) State & prove the De-Margin theorems.
- j) What do you mean by race around condition?
- k) Explain the term LOCKOUT with the help of a suitable example?
- 1) What is the difference between Latch and a Flip-Flop?
- m) What is a shift register? What are the various configurations of shift register?
- n) Differentiate between synchronous & asynchronous logical circuits.
- o) Explain the operation of master-Slave Flip-flop?

### **Section - B**

 $(9\times 5=45)$ 

- **Q2)** What do you mean by error detecting and correcting codes? Explain both with the help of suitable examples.
- Q3) Obtain the truth table of the following & implement it by using NAND Gates?  $F(A,B,C) = (A \overline{B} + BC)(AC + B \overline{C})$
- **Q4)** Minimize the following Using K-Map and Realize it with NAND Gates?  $F(A,B,C,D) = \sum m(2,3,4,5,1315) + \sum d(8,9,10,11)$
- **Q5)** Implement BCD to Excess-3 Code converter?
- **Q6)** Explain the following terms with help of suitable examples:
  - (a) HAZARDS.
  - (b) RACES.
- Q7) Implement following using 4X16 Decoder.

$$F = X Y + \overline{Z}$$

- **Q8)** What do you mean by Multiplexer. Draw the block diagram and logical diagram of 4:1 Multiplexer.
- **Q9)** Design a synchronous counter using JK flip-flop for the following sequence? 000,101,110,111,011,010,000
- Q10) Explain the term universal shift register.
- *Q11*)Classify the counters and Discuss the BCD Counters. Also explain Ring counters.
- Q12) Explain the various rules of k-map reduction technique.
- Q13) Give any five differences between combinational & sequential logical circuits.

